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09/477,093	01/04/2000	DANIEL W. GREEN	P04237	8705

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EXAMINER	
HARKNESS, CHARLES A	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,093	GREEN, DANIEL W.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004, paper number 20*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,9 and 17 are rejected under 35 U.S.C. 102(b) as being unpatentable over Witt U.S. Patent No. 6,141,747 (herein referred to as Witt). Referring to claims 1,9 and 17, Witt has taught a data processor comprising:

At least one pipelined integer execution unit (Witt column10 lines 66-67, column 11 lines 1-5 and column 10 lines 15-17);

A data cache (Witt column 3 line 62 and figure 1 reference number 44);

An instruction cache (Witt column 3 lines 55-56 and figure 1 reference number 14);

And a floating point unit comprising:

plurality of processing units capable of executing instructions that write operands to an external memory and capable of executing instructions that read operands from said external memory (Witt column 10 lines 66-67, column 11 lines 1-5, and figure 1 reference numbers 40A and 40B). Where it is understood that Execution Core 0 (40A) and Execution Core 1 (40B) from figure 1, contain a plurality of floating point units.

3. An operand queue capable of storing a plurality of operands associated with one or more operations being processed in said floating point unit, wherein said operand queue stores a first operand being written to an external memory by a write instruction executed by a first one of

said plurality of processing units (Witt column 12 lines 19-27 and figure 2 reference number 64) and wherein said operand queue supplies said first operand to a read instruction executed by a second one of said plurality of processing units (Witt column 12 lines 38-56 and column 2 lines 2-7) when said floating point read instruction requires said first operand (Witt figures 1-3, column 14 lines 19-29 and lines 38-56),

wherein said first operand is written to a buffer for storage in an external memory, and wherein a second operand is written directly to the buffer bypassing the operand queue (Witt figure 1, figure 2 numbers 60, 64, column 13 lines 5-56, column 12 lines 38-56; the store ROPs are stored in the store queue and the load/store queue 60 if a miss occurs in the data cache for a cache fill from the external interface unit; the second operand being a load instruction operand will be stored in the load/store queue if a miss occurs, but is not stored in the store queue).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5,10-13 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt in view of Hinton et. al., U.S. Patent No. 5,721,855 (herein referred to as Hinton). Each limitation of claims 1, 9, and 17, from which these claims depend, has been taught in the rejection of claims 1, 9, and 17 above.

6. Referring to claims 2-3,10-11 and 18-19, Witt has not taught wherein said floating point unit further comprises a store conversion unit capable of converting operands in said plurality of floating point processing units from an internal format associated with said plurality of floating point processing units to an external format associated with said external memory. Nor has Witt taught wherein said operand queue receives said first operand from said store conversion unit and transfers said first operand to the external memory. Witt has taught the operand being stored in the load/store queue for transfer of the store operand to an external memory (Witt figure 1, figure 2 numbers 60, 64, column 13 lines 5-56, column 12 lines 38-56). Hinton has taught the use of a store conversion unit capable of converting operands in a floating point processing unit from an internal format associated with said floating point processing unit to the external format associated with said external memory (Hinton column 35, lines 29-39 and figure 25, reference number 2515). Hinton also taught wherein said operand queue receives said first operand from said store conversion unit (Hinton column 35 lines 29-32, and figure 25 reference numbers 2515 and 2535). By using a store conversion unit, the operands can be stored in a standard format while the floating point unit executes the operands in a different format which is optimal for executing. In turn reducing the execution time of the operands, and thus reducing the amount of time required to execute a program. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to add a store conversion unit that transfers the operands to said operand queue, so that the operands can be stored in memory in a different format than which they are executed in the floating point unit.

7. Referring to claims 4-5,12-13, and 20-21 Witt has not taught wherein said floating point unit further comprises a load conversion unit capable of converting incoming operands received

from said external memory from an external format associated with said external memory to an internal format associated with said plurality of floating point processing units. Nor has Witt taught wherein operand queue receives said incoming operands from said external memory and transfers said incoming operands to said load conversion unit. Hinton has taught the use of a load conversion unit capable of converting incoming operands received from an external memory from an external format associated with an external memory to an internal format associated with a floating point processing unit (Hinton column 35 lines 23-28 and figure 25 reference number 2525). Hinton also taught wherein operand queue transfers said incoming operands to said load conversion unit (Hinton figure 25 reference numbers 2535 and 2525). By using a load conversion unit, the floating point unit can access a operand that is in a standard format and then process the operand in its execution unit in a format that optimal for computations, which in turn can speed up the execution time of the operands thus reducing the amount of time required to execute a program. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to add a load conversion unit that receives incoming operands from the operand queue, so that the floating point unit could execute the operands in a different format than which the operands are stored in memory.

8. Claims 6-8, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Witt and Hinton in view of Senter et. al., U.S. Patent No. 5,987,593 (herein referred to as Senter). Each limitation of claims 5 and 13, from which these claims depend, has been taught in the rejection of claims 5 and 13 above.

9. Referring to claims 6-7 and 14-15, the combination of Witt and Hinton has not taught wherein data in said external memory is accessed in groups of N bytes and wherein said floating

point unit further comprises at least one aligner capable of receiving a first incoming operand that is misaligned with respect to a boundary between a first N byte group and a second N byte group and aligning said first incoming operand. Nor has the combination of Witt and Hinton taught wherein said operand queue receives said aligned first incoming operand from said at least one aligner. Senter has taught wherein data in said external memory is accessed in groups of N bytes and wherein said floating point unit further comprises at least one aligner capable of receiving a first incoming operand that is misaligned with respect to a boundary between a first N byte group and a second N byte group and aligning said first incoming operand (Senter column 15 lines 17-64). By aligning the data as it comes into the operand queue, the operand is in proper format to be executed by the floating point execution unit. This allows for operands to be accessed where the data crosses a page boundary without requiring two caches accesses for one load (Senter column 15 lines 31-32). Since one cache access is eliminated the time is reduced for a load instruction, thus reducing the amount of time to execute a program. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use an aligner to align unaligned operands and transferring the results to the operand queue.

10. Referring to claims 8 and 16, the combination of Witt and Hinton has not taught wherein said at least one aligner sets at least one bit in said operand queue to indicate that said aligned first incoming operand is valid. Senter has taught setting at least one bit to indicate that an address is valid (Senter column 9 lines 56-58). By having the aligner set at least one bit in the operand queue in which an operand is stored, the execution unit can check to see if the operand is ready to be executed by checking said at least one bit. This will keep the execution unit from using an invalid operand, which will keep the execution unit from repeating an instruction and

thus reducing the amount of time spent on an instruction, which reduces the time spent executing a program. It would have been obvious to one of ordinary skill in the art at the time of the invention that at least one bit could have been used to show the validity of the operand in the same manner as Senter used at least one bit to show the validity of the address. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have an aligner set at least one bit to indicate the validity of an operand in an operand queue to keep the execution unit from using an invalid operand.

Response to Arguments

11. Applicant's arguments filed 04/19/04, paper number 20, have been fully considered but they are not persuasive.

12. In the remarks, Applicant argues in essence that:

"Witt lacks any mention of writing a 'first operand' stored in an 'operand queue' to a 'buffer for storage in an external memory' and writing a 'second operand' directly to the buffer 'bypassing the operand queue' as recited..."

13. This is not found persuasive. Witt has taught storing the operand of a store instruction in the store queue and then in the load/store queue if a miss occurs in the data cache. Witt has also taught where an operand from a load instruction is stored in the laod/store queue is a data cache miss occurs, but does not store the operand in the store queue (Witt figure 1, figure 2 numbers 60, 64, column 13 lines 5-56, column 12 lines 38-56; the store ROPs are stored in the store queue and the load/store queue 60 if a miss occurs in the data cache for a cache fill from the external interface unit; the second operand being a load instruction operand will be stored in the load/store queue if a miss occurs, but is not stored in the store queue).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness
Examiner
Art Unit 2183
June 10, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100